Amendments to claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

Claim 1 (Currently amended) A driving circuit for a flat display panel, said flat display panel including a display area, comprising:

a plurality of video signal lines for providing video signals;

at least one buffer unit for inverting a scanning signal; and

a plurality of switch units disposed between said plurality of video signal lines, and said plurality of switch units and said display area of said flat display panel being spaced apart with at least one video signal line between the switch units and the display area[[;]],

wherein each of said plurality of switch units is connected to at least one video signal line to receive a video signal and is connected to said buffer unit to receive said scanning signal inverted by said buffer unit, and

~~wherein~~ said scanning signal controls output of said video signals by the plurality of switch units to ~~a~~ said display area of said flat display panel.

Claim 2 (Amended) The driving circuit of claim 1, wherein said video signals include analog video signals. ~~said plurality of switch units and said display area of said flat display panel are spaced apart with at least one video signal line.~~

Claim 3 (Original) The driving circuit of claim 1, wherein said buffer unit for inverting a scanning signal is an inverting circuit receiving a timing signal which is then inverted to output at least one scanning signal.

Claim 4 (Original) The driving circuit of claim 2, wherein said at least one scanning signal is an inversed signal of said timing signal.

Claim 5 (Previously Presented) The driving circuit of claim 1, wherein said plurality of switch units comprise thin-film transistors.

Claim 6 (Previously Presented) The driving circuit of claim 1, wherein said at least one video signal line is disposed between said plurality of switch units and said buffer unit for inverting a scanning signal.

Claim 7 (Previously Presented) The driving circuit of claim 1, wherein said plurality of video signal lines are disposed between said switch units and said display area.

Claim 8 (Previously Presented) The driving circuit of claim 1, wherein said flat display panel comprises a liquid crystal display panel.

Claim 9 (New) A driving circuit for a flat display panel, said flat display panel including a display area, comprising:

a first video signal line for providing video signals;

a second video signal line for providing video signals;

a third video signal line for providing video signals;

at least one buffer unit for inverting a scanning signal;

a first switch unit disposed between said first video signal line and said third video signal line;

a second switch unit disposed between said first video signal line and said third video signal line;

a third switch unit disposed between said first video signal line and said third video signal line, and said first, second, third switch units and said display area of said flat display panel being spaced apart with said third video signal line being between said switch units and said display area; and

wherein said first switch unit is connected to said first video signal line to receive a video signal and is connected to said buffer unit to receive said scanning signal inverted by said buffer unit, said second switch unit is connected to said second video signal line to receive a video signal and is connected to said buffer unit to receive said scanning signal inverted by said buffer unit, said third switch unit is connected to said third video signal line to receive a video signal and is connected to said buffer unit to receive said scanning signal inverted by said buffer unit, and said scanning signal controls output of said video signals by said first switch unit, said second switch unit, and said third switch unit to said display area of said flat display panel.

Claim 10 (New) The driving circuit of claim 9, wherein said video signals includes analog video signals.

Claim 11 (New) The driving circuit of claim 9, wherein said buffer unit for inverting a scanning signal is an inverting circuit receiving a timing signal which is then inverted to output at least one scanning signal.

Claim 12 (New) The driving circuit of claim 10, wherein said at least one scanning signal is an inversed signal of said timing signal.

Claim 13 (New) The driving circuit of claim 9, wherein said first switch unit, said second switch unit, and said third switch unit comprise thin-film transistors.

Claim 14 (New) The driving circuit of claim 9, wherein said first video signal line is disposed between said first switch unit and said buffer unit for inverting a scanning signal.

Claim 15 (New) The driving circuit of claim 9, wherein said third video signal line is disposed between said first, second, third switch units and said display area.

Claim 16 (New) The driving circuit of claim 9, wherein said flat display panel comprises a liquid crystal display panel.